UNIT I
INSTRUCTION LEVEL PARALLELISM

TWO MARK QUESTIONS

1. Differentiate desktop, Embedded and server computers?
2. Define the following terms
   - ✓ Execution time
   - ✓ CPU time
   - ✓ Throughput
3. What are the different levels of program used for evaluating the performance of a machine?
4. What is SPEC?
5. Define Total execution time?
6. State Amdahl's law?
7. Define Speedup?
8. Give the CPU performance equation and define the following
   - ✓ CPI
   - ✓ Instruction count
9. What are the various classes of instruction set architecture?
10. Explain the various methods by which data level parallelism is obtained?
11. Compare RISC and CISC machines?
12. What is pipelining?
13. What are hazards? Mention its types?
14. How data hazards can be minimized?
15. What are structural hazards? How it can be minimized?
16. What are control hazards?
17. What is score boarding?
18. What is latency?
19. What is reservation table?
20. Explain pipeline throughput and efficiency?
21. What is a basic block?
22. What is ILP?
23. What are forwarding and bypassing techniques?
24. What is loop-level parallelism?
25. What are the various dependences? How to overcome it?
26. How to avoid hazards?
27. What are the different name dependences?
28. What is control dependence?
29. What is data dependence?

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30. What is dynamic scheduling? Compare dynamic scheduling with static pipeline scheduling?
31. Differentiate in-order and out-of-order execution of instruction?
32. What is imprecise exception?
33. Explain Tomasulo's algorithm briefly?
34. Explain WAR hazards?
35. Explain WAW hazards?
36. Explain RAW hazards?
37. Give the merits of Tomasulo's algorithm?
38. How to remove control dependences?
39. Compare 1 bit and 2 bit prediction schemes?
40. Give the merits and demerits of 2 bit prediction scheme?
41. What are correlating branch predictors?
42. What is register renaming?
43. What is commit stage?
44. How multiple instruction issue is handled by dynamic scheduling?
45. What are limitations of ILP?
46. What is thread level parallelism (TLP)?
47. What is loop unrolling?

16 MARKS QUESTIONS

1. What is dynamic scheduling? Explain with suitable examples the Tomasulo's algorithm for MIPS processor?
2. What is branch prediction? Explain the various schemes in detail?
3. Explain in detail the hardware based speculation for a MIPS processor? Explain how multiple issue is handled with speculation?
4. Compare Tomasulo's algorithm and hardware based speculation?
5. With suitable illustrative examples, explain how compiler techniques can be exploited for achieving ILP?
6. Explain in detail about static branch prediction.

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UNIT II
MULTIPLE ISSUE PROCESSORS

TWO MARK QUESTIONS

1. Explain static multiple issues with respect to VLIW approach?
2. Compare local scheduling and global scheduling.
3. What is trace scheduling?
4. Discuss the various problems associated with the VLIW processor and measures for their mitigation?
5. What is loop carried dependence and dependence distance?
6. What is the need to detect loop dependences? How does the compiler detect it?
7. What is inter-procedural analysis?
8. What is copy propagation?
9. What is tree height reduction?
10. What are recurrences?
11. Explain software pipelining and trace scheduling. Compare them.
12. What is critical path?
13. Explain the methods involved in trace scheduling.
14. What is superblock?
15. What are predicated instructions? What are its limitations? Give the processors that support conditional move.
16. What are the capabilities required to speculate ambitiously?
17. Mention the methods to speculate ambitiously preserving the exception behavior.
18. What are poison bits?
19. What is a sentinel?
20. What is an IA-64 ISA?
21. What are the various components of IA-64 register model?
22. What is a register stack engine?
23. What is a bundle?
24. What are advanced loads and ALAT?
25. Explain Itanium processor.
26. What are the pipeline stages available in an Itanium processor?

16 MARKS QUESTIONS

1. With an example, explain static multiple issue in a VLIW processor?
2. Explain in detail about multiple issue in a EPIC processor?
3. Explain in detail how compiler support can be used to increase the amount of parallelism that can be exploited in a program.
4. With examples, explain how do you detect and enhance Loop Level Parallelism?
5. Explain software pipelining techniques in detail.

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6. Explain the need for hardware support for exposing more parallelism at compile time.
7. Explain briefly about conditional or predicated instructions and the limiting factors affecting their complete usefulness.
8. Explain compiler speculation with hardware support.
9. Compare Hardware and Software speculation mechanisms.
10. Explain Intel IA-64 Architecture in detail with suitable reference to Itanium processor.
11. Discuss the role of ILP in embedded and mobile applications.

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UNIT III
MULTIPROCESSORS AND THREAD LEVEL PARALLELISM

TWO MARK QUESTIONS

1. Give the taxonomy of parallel architectures.
2. What are the merits of MIMD multiprocessors?
3. What are centralized shared memory architectures and symmetric shared memory multiprocessors?
4. What is distributed shared memory architecture?
5. What is a multicomputer?
6. What are message-passing multiprocessors?
7. What is RPC?
8. What are the performance metrics for communication mechanisms?
9. What are the advantages of different communication mechanisms?
10. What are the major advantages for message passing communication?
11. What are the challenges involved in parallel processing?
12. What are private and shared data?
13. What is multiprocessor Cache Coherence?
14. What is cache coherence problem and when do you say a memory system is coherent? What are cache coherence protocols?
15. What is cache consistency?
16. What is write serialization?
17. What is snooping? What are the various snooping protocols?
18. What are write invalidate and write update protocols?
19. What are the performance differences between write update and write invalidate protocols?
20. What are write through and write back caches?
21. What are ownership misses and coherence misses?
22. Compare true sharing and false sharing misses.
23. What is a directory protocol?
24. What are local node, home node and remote node?
25. What is an atomic exchange?
26. What are the various atomic synchronization primitives?
27. What is load locked and store conditional instructions?
28. What are spin locks?
29. What is barrier synchronization?
30. What is sense-reversing barrier?
31. Explain relaxed consistency models.
32. What is multithreading? Compare its types.
33. What is SMT? What are the design challenges in SMT processors?

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34. What are the potential advantages from SMT?

16 MARKS QUESTIONS

1. Explain in detail the symmetric shared memory architectures with reference to multiprocessor cache coherence problem.
2. Explain in detail the schemes available for enforcing coherence. Discuss its implementation techniques with suitable state diagrams.
3. With relevant graphs, discuss the performance of symmetric shared-memory multiprocessors for various workloads.
4. Explain in detail the distributed shared memory architecture highlighting the directory based cache coherence protocol. Substantiate your explanation with suitable examples and state diagrams.
5. With relevant graphs, discuss the performance of distributed shared memory multiprocessors.
6. Explain in detail the need for synchronization and how it is achieved in a multiprocessor? Discuss the associated implementation issues.
7. Discuss the synchronization mechanisms for larger scale multiprocessors.
8. Explain in detail the memory consistency models.

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UNIT IV
MEMORY AND I/O

TWO MARK QUESTIONS

1. Define the terms: Cache, Cache hit and Cache miss, Miss Rate and Miss penalty.
2. Compare temporal and spatial locality.
3. What are the four common questions for the first level of memory hierarchy? Summarize their solutions.
4. What is a valid bit with reference to cache?
5. Define the terms: Block address and Block offset, Tag and Index field.
6. What is a LRU algorithm?
7. Compare write through and write back.
8. What is a dirty bit?
9. What are the two options available on a write miss?
10. How do you calculate the width of index field for a set associative cache?
11. What is a victim buffer?
12. What is average memory access time and give its formula?
13. Give the relation between average memory access time and processor performance.
14. How to reduce cache miss penalty? What are the various optimizations available?
15. What is multilevel inclusion?
16. What are critical word first and early restart techniques?
17. Should read misses be given priority over writes? Comment.
18. What is write merging?
19. What is a victim cache?
20. How to reduce miss rate? Categorize misses.
21. How miss rates improve with higher associativity?
22. What is 2:1 cache rule of thumb?
23. What are way prediction and pseudo associative caches?
24. What is a virtual cache?
25. Explain the various techniques available for improving the performance of main memory.
26. How does interleaving improve the performance of a main memory unit? What is interleaving factor?
27. How do you determine the number of banks for main memory? What are the demerits memory banks?
28. How do independent memory banks support higher bandwidth for main memory?
29. Compare access time and cycle time.
30. Compare DRAM and SRAM.
31. What is DIMM?
32. What is SDRAM?

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33. What is RAMBUS, RDRAM and DRDRAM?
34. Compare RAMBUS and DDR SDRAM.
35. What is virtual memory?
36. How does the cache and virtual memory differ?
37. What are pages, segments and paged segments with respect to virtual memory?
38. Where can a block be placed in main memory?
39. How is a block found if it is in main memory?
40. What is a page table and inverted page table?
41. What is a translation lookaside buffer?
42. Which block should be replaced on a virtual memory miss?
43. What is a use bit?
44. What happens on a write in main memory?
45. Explain the techniques for fast address translation.
46. What are the different storage devices available?
47. Define the terms: (a) Seek time (b) Rotational latency with reference to hard disk?
48. How do you compute area density of magnetic disk?
49. What is a Flash memory?
50. What is split transaction?
51. What are the various bus standards available?
52. What is Reliability, Availability and Dependability with reference to storage systems?
53. What is module reliability and module availability with reference to storage systems?
54. What is mirroring?
55. What is bit interleaved parity and block interleaved parity?
56. What is P+Q redundancy?
57. How do you measure I/O performance?
58. Compare Throughput vs Response time?

16 MARKS QUESTIONS

1. Describe in detail how the four memory hierarchical questions can be handled? Illustrate the answers with an example.
2. Explain how cache performance is measured and how it can be improved?
3. Discuss in detail the various techniques available for reducing cache miss penalty?
4. Discuss how cache behavior can be improved by reducing the miss rate?
5. Discuss how reducing cache miss penalty or miss rate by parallelism would provide scope for performance improvement in a memory module?
6. Explain how reducing hit time in a cache would speedup the memory module?
7. Describe in detail how performance improvement of main memory could be targeted?
8. Elaborate on the various memory technologies that you know and give a comparative study.

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9. Explain the paged and segmented virtual memory protections each with a suitable example. Compare them.
10. Discuss in detail the various types of storage devices.
11. Explain the Bus standards and the interfaces. With timing diagrams, explain the read and write operations occurring in a typical bus.
12. Discuss Reliability, Availability and Dependability for storage devices in detail.
13. Explain RAID architecture in detail.
14. Explain in detail how I/O performance of storage systems can be measured?
15. Describe in detail the process involved in designing an I/O system.

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UNIT V
MULTI-CORE ARCHITECTURES

TWO MARK QUESTIONS

1. What is Simultaneous multithreading?
2. What are multiprocessors? Mention the categories of multiprocessors?
3. What is multitasking? Explain about Multithreading?
4. Write the advantages of Multithreading.
5. Write the disadvantages of Multithreading.
6. Define Software Multithreading
7. Define Hardware Multithreading
8. List some advantages of Software Multithreading.
9. What is CMT?
10. What is SMT?
11. What are the Disadvantages of SMT?
12. What is a Heterogeneous Multi-core processor?
13. Write the advantages of heterogeneous multi core architectures?
14. Explain about IBM Cell Processor architecture.
15. List the components of IBM cell architecture
16. What are the components of PPE?
17. What is Memory Flow Controller (MFC)?
18. What is multicore'?
19. Write the software implications of a multicore processor?
20. What is fine grained multithreading?
21. What is coarse grained multithreading?
22. What is a cell processor?
23. What is the function of Power Processing Unit?
24. List out the disadvantages of Heterogeneous multi-core processors?
25. What is hyper threading and HT Technology?
26. What are the various processor configurations?
27. What happens to a superscalar without multithreading support?
28. What are the design challenges in SMT?

16 MARKS QUESTIONS

1. Explain in Detail about Multicore architectures?
2. Discuss in detail about the applications benefit from multicore?
3. Explain in detail about software multithreading?
4. Discuss Flynn's taxonomy?
5. Explain in detail about hardware multithreading techniques?
6. Explain in detail about CMP architecture and SMT architecture?
7. Discuss the design issues of CMP and SMT architecture?

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8. Discuss about Intel multi-core architecture?
9. Describe in detail about SUN CMP architecture
10. Discuss in detail about heterogeneous multi-core processors?
11. Explain about IBM Cell Processor?

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